CLAIMS

1. An automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

automatically enlarging a spacing between neighboring features of a path of a layout provided that the length of the path does not then exceed a predetermined dimensional constraint and provided that connectivity is maintained between the neighboring features and any features of the layout to which the neighboring features are connected; and

repeating said enlarging for at least one other spacing of the layout.

2. A method of de-compacting a layout as claimed in claim 1 wherein said enlarging is repeated until all enlargeable spacings of said layout are enlarged.

3. A method of de-compacting a layout as claimed in claim 2 wherein said spacings are enlarged in order from a smallest said spacing of said layout.

4. A method of de-compacting a layout as claimed in claim 1 wherein said predetermined dimensional constraint is a critical path length (C) of said layout in a first direction of said layout.

5. A method of de-compacting a layout as claimed in claim 1 wherein said predetermined dimensional constraint represents a dimension of an area available for said layout in a first direction.

6. A method of de-compacting a layout as claimed in claim 2 wherein said predetermined dimensional constraint limits the length of said path in a first direction of the layout, wherein said neighboring features include a first feature and a second feature neighboring said first feature of said spacing, wherein said path includes a first neighbor spacing between said first feature and a third feature neighboring said first feature, and when said path includes a fourth feature neighboring said second feature, said path further includes a second neighbor spacing between said second feature and said fourth feature,

wherein said spacing is enlarged only when said spacing is smaller than the larger of said first neighbor spacing and said second neighbor spacing by a predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said spacing is enlarged only when said spacing is smaller than said first neighbor spacing by said predetermined amount.

7. A method of de-compacting a layout as claimed in claim 6 wherein when said spacing is enlarged, said spacing is enlarged by said predetermined amount.

8. A method of de-compacting a layout as claimed in claim 7 wherein when said spacing is enlarged, the larger of said first neighbor spacing and said second neighbor spacing is reduced by said predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said first neighbor spacing is reduced by said predetermined amount.

9. A method as claimed in claim 8 wherein each said spacing is enlarged as many times as enlargeable.

10. A method of decompacting a layout of a portion of an integrated circuit, comprising:

a) providing a predetermined dimensional constraint for said layout in a first direction of said layout;

b) automatically enlarging a spacing between first and second features of a path of said layout by a predetermined amount, provided that the length of said path does not then exceed said predetermined dimensional constraint and provided that connectivity is maintained between said first and second features and any features of the layout to which said first and second features are connected, when said spacing is smaller by said predetermined amount than the larger of a first neighbor spacing between said first feature and a third feature of said path neighboring said first feature, and a second neighbor spacing between said second feature and a fourth feature of said path neighboring said second feature; and

c) repeating said step b) in order from a smallest said spacing enlargeable by said step b) until all spacings enlargeable by said step b) are enlarged as many times as enlargeable.

11. A machine-readable medium recording a set of instructions for performing a method of decompacting a layout for a portion of an integrated circuit, said method comprising:

automatically enlarging a spacing between neighboring features of a path of a layout provided that the length of the path does not then exceed a predetermined dimensional constraint and provided that connectivity is

maintained between the neighboring features and any features of the layout to which the neighboring features are connected; and

repeating said enlarging for at least one other spacing of the layout.

12. A machine-readable medium as claimed in claim 11, wherein said enlarging is repeated until all enlargeable spacings of said layout are enlarged.

13. A machine-readable medium as claimed in claim 12, wherein said spacings are enlarged in order from a smallest said spacing of said layout.

14. A machine-readable medium as claimed in claim 11, wherein said predetermined dimensional constraint is a critical path length (C) of said layout in a first direction of said layout.

15. A machine-readable medium as claimed in claim 11, wherein said predetermined dimensional constraint represents a dimension of an area available for said layout in a first direction.

16. A machine-readable medium as claimed in claim 12, wherein said predetermined dimensional constraint limits the length of said path in a first direction of the layout, wherein said neighboring features include a first feature and a second feature neighboring said first feature of said spacing, wherein said path includes a first neighbor spacing between said first feature and a third feature neighboring said first feature, and when said path includes a fourth feature neighboring said second feature, said path

further includes a second neighbor spacing between said second feature and said fourth feature,

wherein said spacing is enlarged only when said spacing is smaller than the larger of said first neighbor spacing and said second neighbor spacing by a predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said spacing is enlarged only when said spacing is smaller than said first neighbor spacing by said predetermined amount.

17. A machine-readable medium as claimed in claim 16, wherein when said spacing is enlarged, said spacing is enlarged by said predetermined amount.

18. A machine-readable medium as claimed in claim 17, wherein when said spacing is enlarged, the larger of said first neighbor spacing and said second neighbor spacing is reduced by said predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said first neighbor spacing is reduced by said predetermined amount.

19. A machine-readable medium as claimed in claim 18, wherein each said spacing is enlarged as many times as enlargeable.

20. A machine-readable medium recording a set of instructions for performing a method of decompacting a layout of a portion of an integrated circuit, said method comprising:

a) providing a predetermined dimensional constraint for said layout in a first direction of said layout;

b) automatically enlarging a spacing between first and second features of a path of said layout by a predetermined amount, provided that the length of said path does not then exceed said predetermined dimensional constraint and provided that connectivity is maintained between said first and second features and any features of the layout to which said first and second features are connected, when said spacing is smaller by said predetermined amount than the larger of a first neighbor spacing between said first feature and a third feature of said path neighboring said first feature, and a second neighbor spacing between said second feature and a fourth feature of said path neighboring said second feature; and

c) repeating said step b) in order from a smallest said spacing enlargeable by said step b) until all spacings enlargeable by said step b) are enlarged as many times as enlargeable.

21. A system operable to decompact a layout for a portion of an integrated circuit, said system comprising:

a processor operable to automatically enlarge a spacing between neighboring features of a path of a layout provided that the length of the path does not then exceed a predetermined dimensional constraint and provided that connectivity is maintained between the neighboring features and any features of the layout to which the neighboring features are connected, said processor further being operable to repeat said enlarging for at least one other spacing of the layout.

22. A system as claimed in claim 21 wherein said processor is further operable to repeat said enlarging until all enlargeable spacings of said layout are enlarged.

23. A system as claimed in claim 22 wherein said processor is further operable to enlarge said spacings in order from a smallest said spacing of said layout.

24. A system as claimed in claim 21 wherein said predetermined dimensional constraint is a critical path length C of said layout in a first direction of said layout.

25. A system as claimed in claim 21 wherein said predetermined dimensional constraint represents a dimension of an area available for said layout in a first direction.

26. A system as claimed in claim 22 wherein said predetermined dimensional constraint limits the length of said path in a first direction of the layout, wherein said neighboring features include a first feature and a second feature neighboring said first feature of said spacing, wherein said path includes a first neighbor spacing between said first feature and a third feature neighboring said first feature, and when said path includes a fourth feature neighboring said second feature, said path further includes a second neighbor spacing between said second feature and said fourth feature,

wherein said processor is operable to enlarge said spacing only when said spacing is smaller than the larger of said first neighbor spacing and said second neighbor spacing by a predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said processor is operable to enlarge said spacing only when said spacing is smaller than said first neighbor spacing by said predetermined amount.

27. A system as claimed in claim 26 wherein said processor is operable to enlarge said spacing by said predetermined amount.

28. A system as claimed in claim 27 wherein when said spacing is enlarged by said processor, said processor is further operable to reduce the larger of said first neighbor spacing and said second neighbor spacing by said predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said processor is operable to reduce said first neighbor spacing by said predetermined amount.

29. A system as claimed in claim 28 wherein said processor is further operable to enlarge each said spacing as many times as said spacing is enlargeable.

30. A system operable to de-compact a layout for a portion of an integrated circuit, said system comprising:

a processor operable to automatically enlarge a spacing between first and second features of a path of said layout by a predetermined amount, provided that the length of said path does not then exceed a predetermined dimensional constraint for said layout and provided that connectivity is maintained between said first and second features and any features of the layout to which said first and second features are connected, when said spacing is smaller by said predetermined amount than the larger of a first neighbor spacing between said first feature and a third feature of said path neighboring said first feature, and a second neighbor spacing between said second feature

and a fourth feature of said path neighboring said second feature,

wherein said processor is further operable to automatically enlarge a plurality of said spacings of said layout in order from a smallest said spacing until all said spacings enlargeable by said processor are enlarged as many times as enlargeable.